# InGaAs revolutionizes III-V MOSFETs

Several decades of research have failed to boost the tiny currents in inversion-mode III-V MOSFETs. However, massive improvements are possible by combining indium-rich InGaAs channels with high-k dielectrics grown by atomic-layer-deposition, explains **Peide Ye** from Purdue University.

It's impossible to deny that silicon is an incredibly successful semiconductor because it forms the key ingredient in a microelectronics industry worth more than $500 billion a year. However, this material still has its weaknesses, and its MOSFETs are limited by their relatively slow mobility. III-Vs, such as GaAs, InSb and InAs, are substantially better in this regard, and this advantage has fueled more than 40 years of development of a compound semiconductor MOSFET. These decades of research have produced several minor successes, but any real progress has been held back by the complexities associated with unraveling the physics and chemistry of compound semiconductor surfaces and interfaces.

The story of the III-V MOSFET began in 1965, when the Radio Corporation of America announced that it had built the first GaAs MOSFET. This transistor produced a very low current, so efforts were soon under way to boost this key characteristic. $SiO_2$ was quickly discarded as a good gate dielectric for GaAs and since then the search has been on for low-defect, thermodynamically stable alternatives.

The most significant advances have occurred approximately every 10 years and have focused on GaAs MOSFETs. Initial breakthroughs included the development of pyrolytically deposited silicon dioxide, silicon nitride, silicon oxynitride and aluminum oxide in the 1970s. Sulphur passivation followed in 1987, which improved the device by cutting the GaAs surface recombination velocity, and 1996 saw the introduction of $Ga_2O_3$ and $Gd_2O_3$ oxides. These films produce good-quality interfaces, but require a multichamber MBE technique that is unsuitable for high-volume manufacturing.

PEIDE YE

**Peide Ye's team at Purdue University** is producing inversion-mode InGaAs MOSFETs with minority carrier currents of more than 1 A/mm. These transistors feature gates made from $Al_2O_3$, $HfO_2$ and HfAlO dielectrics, which are grown by atomic-layer-deposition in an ASM ALD F-120.

### Recent advances

We have now entered the fifth era of advancement for III-V MOSFETs. This has been led by Intel, which is seeking alternative technologies beyond silicon CMOS. These could include germanium, III-Vs, carbon nanotubes and possibly graphene.

Today's efforts on III-V MOSFETs have expanded beyond GaAs and can be subdivided into those based on arsenides, phosphides, nitrides and antimonides. These compounds have a wide range of bandgaps and carrier mobilities, so they are suited to different applications.

The antimonides, a material system that Intel has been working on in collaboration with the UK defense and technology company Qinetiq, is well suited to high-speed, low-power digital applications. High mobilities are the key here and InSb devices can deliver electron mobilities of 77,000 $cm^2/Vs$.

Phosphides are also suitable for logic applications, whereas GaN-based MOSFETs could potentially improve the output power, dynamic swing and reliability for RF power applications. Meanwhile, GaAs-based MOSFETs promise to deliver higher mobilities and higher breakdown voltages than the silicon LDMOSFETs that are currently being employed in wireless base stations.

The lack of progress made with all types of III-V MOSFET stems from their relatively poor interfaces. Silicon is blessed with a high-quality, thermodynamically stable native oxide that produces very little carrier trapping – its mid-bandgap interface-trap density is typically just $10^{10}/cm^2$-eV. The quality of this interface results from the passivation of 99.999% of the surface's dangling bonds.

This very high degree of passivation must be

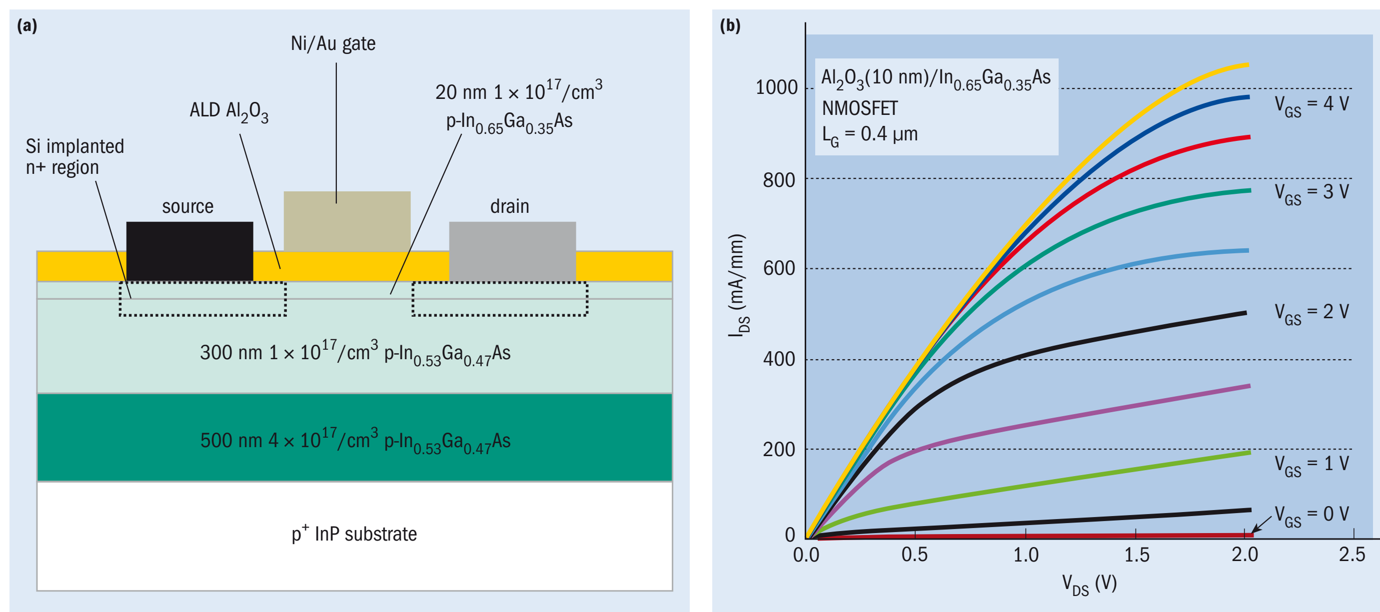



**Fig. 1.** Switching the GaAs to InGaAs has been the key to improving III-V MOSFETs **(a)**. Current-voltage curves **(b)** show that the inversion-type E-mode $In_{0.65}Ga_{0.35}As$ MOSFET is normally off at zero bias, which makes it suitable for digital applications. This transistor has a 10 nm thick $Al_2O_3$ gate dielectric and a 0.4 µm gate length.

replicated in the III-Vs if they are to deliver a similar performance to their silicon cousins. However, this is a real challenge for compound semiconductors because their native oxide is far more complicated. In the case of GaAs, it is a leaky and defective mixture of $Ga_2O_3$, $As_2O_3$ and $As_2O_5$. Such a material causes pinning of the Fermi level, which nullifies the device performance by preventing any bending of the surface potential.

Finding a material that perfectly passivates all of the dangling bonds of gallium and arsenic is a real challenge. Decades of effort in industry and academia has focused on this very problem, which has involved attempts to demonstrate a GaAs MOSFET working under inversion operation – the configuration that's suited to digital applications and employed in silicon. However, all of the researchers have had very little to show for their toil and have tended to turn their back on this field after only producing poor-performing transistors. High currents are a key measure of device quality and these versions have only delivered in the nanoamp or microamp range. This lack of success has left a bad legacy – even today young researchers tend to avoid this field after hearing scare stories of years of effort lost to Fermi level pinning.

The interface issue doesn't just plague III-Vs – it is starting to become something of a headache for silicon. That's because the dielectric properties of silicon dioxide are not good enough for CMOS at the 45 nm node, which has forced this community to search for other compounds that could provide a high-k dielectric solution.

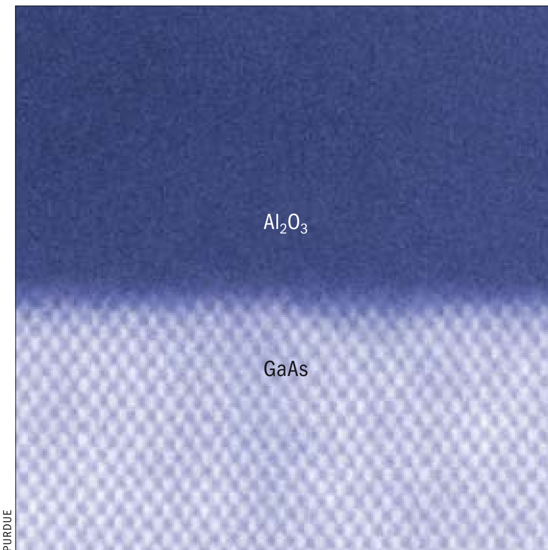
Well funded research in this field began in the late 1990s and has had great success. It is now possible to deposit high-k dielectrics on silicon using atomic-layer-deposition (ALD), a technique that involves the growth of a single-atomic layer of one element, followed by purging of the growth chamber and growth of a second single-atomic layer of another element. Purging follows again and the growth is repeated to form a film. This approach is now a manufacturable technology that can be applied to the 45 nm CMOS node and beyond.

## Borrowing from silicon technology

At the end of 2001, while working at Bell Labs/Agere Systems in Murray Hill, NJ, I applied ALD to III-V devices. This was carried out in collaboration with my colleague Glen Wilk, in the same building where the transistor was first invented, and involved the growth of MOS structures with high-k dielectrics $Al_2O_3$ and $HfO_2$.

We got off to a great start, with a shocking but very pleasing result. Our first GaAs capacitor – which was fabricated to evaluate interface quality – produced channel modulation, even though it was grown without the prior removal of the native oxide. The reasons behind this success are now understood, because ALD has been shown to produce a "self-cleaning" effect, according to researchers at various institutions including IBM, Rutgers, the National Tsinghwa University in Taiwan, the University of Texas in Dallas and the University of Texas in Austin.

The early successes with ALD sparked a dramatic growth of the III-V MOSFET community, which now includes many leading universities and the industrial giants Intel and IBM. However, transistor currents are still languishing in the 1–100 µA range when operated in the inversion-mode configuration that is required for digital applications (this mode of operation involves the generation of a minority carrier current between the source and drain, which




**An abrupt transition occurs** between the GaAs and $Al_2O_3$ layers grown by atomic-layer-deposition at 300 °C, according to cross-sectional high-resolution transmission electron images. The native oxide is etched away by ALD's "self-cleaning" process.

is introduced by the field-effect from the gate bias). These currents are hardly any better than those reported 20 or 30 years ago.

However, vast improvements are possible by employing an InGaAs channel, rather than one made from GaAs, according to research by myself and my colleague Yi Xuan. In 2005 we started to work with InGaAs – a ternary alloy that is already being employed for the conduction channel in GaAs PHEMTs and InP HEMTs. The bandgap of this ternary can be reduced from 1.42 eV (no indium content) to 0.36 eV (no gallium content), which improves characteristics such as mobility and saturation velocity.

We have built a range of inversion-mode surface channel $In_xGa_{1-x}As$ MOSFETs with an indium content, *x*, of 20, 53 and 65%. These transistors, which contain $Al_2O_3$, $HfO_2$ and HfAlO dielectrics deposited by ALD, behave in the same way as silicon MOSFETs, but are expected to show a far higher mobility. The version with the least amount of indium produces a current of 1 mA/mm, but this rockets to 0.4 A/mm and more than 1 A/mm for MOSFETs with an indium content of 53 and 65%, respectively. Our $In_{0.65}Ga_{0.35}As$ transistor is the first III-V surface channel MOSFET that is a real field-effect device with an inversion current of more than 1 A/mm. It even exceeds the upper measurement limit for a standard semiconductor parameter analyzer, which is 100 mA for a 100 µm wide device.

The performance of our 0.4 µm gate length $Al_2O_3$/$In_{0.65}Ga_{0.35}As$ MOSFET, which has a conduction channel directly underneath the high-k dielectric, is shown in figure 1. The DC current-voltage characteristics show the variations in the inversion current with gate bias. It is suitable for digital applications because it is normally off at zero bias. Turning it on at a positive gate bias provides a drain current of 1.05 A/mm. This drain current is far higher than GaAs PHEMTs and InP HEMTs, and comparable to GaN HEMTs grown on SiC.

Our device's most promising characteristic is its ability to scale down to a submicron gate length. Hopefully this scaling will continue down to the length scales associated with silicon MOSFETs, because this would lead to 10 A/mm or 10 mA/µm III-V MOSFETs at a III-V 45 nm technology node.

Our III-V MOSFET is in its infancy and there is a lot to learn regarding materials, structures and devices. However, we believe that our advances have resulted from an $In_{0.65}Ga_{0.35}As$ channel that has a very high electron mobility and saturation velocity.

We have found that the changes in surface potential for strong inversion are much less for InGaAs channels than those made from GaAs. More importantly, $In_{0.65}Ga_{0.35}As$ has a charge neutrality level that is typically just 0.15 eV less than the conduction band minimum. This prevents the build up of a large number of negative trapped charges at the interface, which can inhibit the introduction of additional inversion carriers by the field effect.

One of our next goals is to cut the mid-bandgap interface-trap density to $10^9$–$10^{10}$/$cm^2$-eV. Our current ALD-based process can reduce this density to $10^{11}$–$10^{12}$/$cm^2$-eV, which equates to the passivation of 999 dangling bonds out of 1000. But a manufacturable III-V MOSFET technology demands passivation of 99,999 dangling bonds out of 100,000.

**Applications in the community**

The silicon CMOS community, which is looking for an alternative device technology for high-speed low-power digital applications, is likely to welcome the introduction of III-V MOSFETs. However, they will insist that they can be produced on silicon wafers of at least 300 mm in diameter. But there may well be a time when it is possible to locally grow germanium and InGaAs on silicon. This could form germanium PMOSFETs and InGaAs NMOSFETs, the building blocks for a new generation of CMOS that still employs silicon substrates, but is not held back by this material's low mobility. However, before we get carried away, we must remember that there is still plenty of work to do to make silicon, germanium and the III-Vs happy bedfellows.

There are also some other potential applications for our high-performance InGaAs MOSFETs. This device could serve low-power RF applications that are less demanding on interface quality. These surface channel MOSFETs can deliver a low gate leakage, large dynamic swing and high linearity.

I am optimistic about the future and I hope that the progress of III-Vs in the silicon CMOS community will parallel that of the high-k dielectrics that were introduced in the late 1990s. That technology is now paying dividends for chip manufacturers and hopefully the III-V MOSFET can follow that path over the next few years.

**About the author**

**Peide (Peter) Ye** has been an associate professor of electrical and computer engineering at Purdue University since 2005. He previously spent four years at Bell Labs of Lucent Technologies and Agere Systems in Murray Hill, NJ, where he pioneered an atomic-layer-deposition process on III-Vs. His current research focuses on high-k integration with novel channel materials for device applications. He thanks the US National Science Foundation and the Semiconductor Research Corporation Focus Center Research Program for funding his current research.